

**WHAT IS CLAIMED IS:**

1. In a phase locked loop system, a digitally-synthesized loop filter circuit comprising:
  - a first circuit for providing a digital representation of a phase error signal of the phase locked loop;
  - a second circuit responsive to the digital phase error signal, for generating a multi-bit accumulated digital phase error signal representing an accumulated value of successive values of the digital phase error signal; and
  - a third circuit for generating an output signal corresponding to the accumulated digital phase error signal, said output signal useful for controlling an oscillator within the phase locked loop.
2. The invention defined by claim 1 wherein the first circuit comprises:
  - a digital phase detector circuit for the phase locked loop system.
3. The invention defined by claim 2 wherein the digital phase error signal comprises:
  - a quantized-time and quantized-value signal which encodes polarity of phase error.
4. The invention defined by claim 2 wherein the digital phase error signal comprises:
  - a quantized-time and quantized-value signal which linearly encodes phase error.
5. The invention defined by claim 1 wherein the first circuit comprises:
  - an analog-to-digital converter circuit for converting an analog representation of a phase error signal into a corresponding digital representation.
6. The invention defined by claim 5 wherein the first circuit comprises:
  - a delta-sigma encoder circuit having a clock input coupled to receive a first clock signal.

7. The invention defined by claim 1 wherein the second circuit comprises:  
a digital accumulator circuit for accumulating successive values of a digital  
input signal representing the phase error, and for providing on an  
output thereof a multi-bit accumulated digital phase error signal.

8. The invention defined by claim 7 wherein the digital accumulator circuit  
comprises:

an accumulator circuit for conveying the multi-bit accumulated digital phase  
error signal having a variable number of bits beginning with the least  
significant bit.

9. The invention defined by claim 7 wherein the digital accumulator circuit  
comprises:

a lower-order accumulator circuit having an input responsive to the digital  
input signal representing the phase error, and having at least one  
output; and  
an upper-order accumulator circuit having an input coupled to an output of the  
lower-order accumulator circuit, and having an output for conveying a  
portion of the multi-bit accumulated digital phase error signal;  
wherein both the lower-order accumulator circuit and the upper-order  
accumulator circuit together compute the multi-bit accumulated digital  
phase error signal.

10. The invention defined by claim 9 wherein:  
the upper-order accumulator circuit is clocked at a lower rate than the lower-  
order accumulator circuit is clocked.

11. The invention defined by claim 9 wherein:  
of the upper-order and lower-order accumulator bits forming the accumulated  
digital phase error signal, only a portion of the bits are conveyed to the  
third circuit.

12. The invention defined by claim 11 wherein:

of the upper-order and lower-order accumulator bits forming the accumulated digital phase error signal, only upper-order accumulator bits are conveyed to the third circuit.

13. The invention defined by claim 7 wherein:

the digital phase error signal from the first circuit is coupled to the digital accumulator circuit as the digital input signal.

14. The invention defined by claim 13 wherein the second circuit comprises:

a digital accumulator circuit having an input coupled to receive the digital phase error signal, having a clock input coupled to receive an accumulator clock signal, and having an output for conveying a multi-bit output signal representing an accumulated value of successive values of the digital phase error signal.

15. The invention defined by claim 7 wherein:

the digital input signal for the digital accumulator circuit is derived from the digital phase error signal received from the first circuit.

16. The invention defined by claim 15 wherein the second circuit further

comprises:

a decimator circuit responsive to the digital phase error signal, for generating a decimated digital phase error signal which is coupled to the accumulator circuit as the digital input signal.

17. The invention defined by claim 1 wherein:

the output signal comprises an analog representation of at least a most-significant-bit portion of the accumulated digital phase error signal.

18. The invention defined by claim 1 wherein:

the multi-bit accumulated digital phase error signal is computed to a greater number of bits than is conveyed to the third circuit.

19. The invention defined by claim 1 wherein the third circuit comprises:

a digital-to-analog converter circuit.

20. The invention defined by claim 19 wherein the third circuit further comprises:

a low-pass filter circuit connected to an output of the digital-to-analog converter circuit.

21. The invention defined by claim 1 wherein:

an effective value of capacitance provided by the digitally-synthesized loop filter circuit increases with increasing numbers of bits in the accumulated digital phase error signal.

22. The invention defined by claim 21 wherein:

the number of bits in the accumulated digital phase error signal is configurable.

23. The invention defined by claim 22 wherein:

the number of bits in the accumulated digital phase error signal is configurable to alter an operating characteristic of the phase locked loop system.

24. The invention defined by claim 1 wherein:

the loop filter circuit is implemented entirely within an integrated circuit.

25. The invention defined by claim 1 wherein:

the loop filter is implemented entirely within an integrated circuit configured to recover clock and data from an incoming data signal having more than one possible data rate; and

the number of bits in the accumulated digital phase error signal is configurable based upon the data rate of the incoming data input signal.

26. The invention defined by claim 1 wherein:

the first circuit comprises a digital encoder circuit forming a portion of a phase detector circuit for the phase locked loop system, said digital encoder circuit having a clock input coupled to receive a first clock signal.

27. The invention defined by claim 26 wherein the second circuit comprises:  
a decimator circuit responsive to the digital phase error signal from the first circuit, for generating a decimated digital phase error signal having a lower data rate than the digital phase error signal; and  
a digital accumulator circuit for accumulating successive values of the decimated phase error signal, having a clock input coupled to receive a second clock signal having a clock rate lower than that of the first clock signal, and for providing on an output thereof at least a most-significant-bit portion of the multi-bit accumulated digital phase error signal.
28. The invention defined by claim 27 wherein the third circuit comprises:  
a digital-to-analog converter circuit having an input responsive to at least the most-significant-bit portion of the multi-bit accumulated digital phase error signal, and having an output; and  
a filter having an input connected to the output of the digital-to-analog converter circuit, and having an output for providing the output signal corresponding to the accumulated digital phase error signal.